

IN THE SPECIFICATION

Please amend the Abstract as follows:

--This invention has as its object to suppress an increase in circuit scale and to simplify a circuit structure by executing a filter process using a plurality of arithmetic units each of which makes multiplication and addition. To achieve this object, image data Y_{n+2} , Y_{n+3} , and Y_{n+4} to be processed are read out (S2901), and three lattice point data $d'n+l$, $S'n$, and $dn-1$ are respectively read out from sequences H1, H2, and H3 corresponding to line buffers that store the lattice point data (S2903). $d'n+3 = Y_{n+3} + \alpha (Y_{n+2} + Y_{n+4})$ is computed (S2905), and $d'n+3$ is stored in the sequence H1 (S2907). $S'n+2 + \beta (d'n+l + d'n+3)$ is computed (S2909), and $S'n+2$ is stored in the sequence H2 (S2911). $d'n+l = d'n+l + y(S'n+2 + S'n)$ is computed (S2913), and $dn+l$ is stored in the sequence H3 (S2915). $Sn = S'n + \delta (dn-1 + dn+l)$ is computed (S2917), and Sn and $dn+l$ are output to the next processing stage (S2919).--